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EXAMINER	
NGUYEN, MICHELLE P	
ART UNIT	PAPER NUMBER
2851	

DATE MAILED: 08/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/973,231	SINGH ET AL.	
	Examin r	Art Unit	
	Michelle Nguyen	2851	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The disclosure is objected to because:

(a) It does not include a detailed description about Fig. 25.

(b) On page 10, line 2, "light reflected from the wafer 34" should be --light 34 reflected from the wafer--.

Appropriate correction is required.

Drawings

2. The drawings are objected to because:

(a) They fail to comply with 37 CFR 1.84(p)(4) because reference characters "1724" and "1726" have both been used to designate the same layer (see Fig. 24).

(b) They fail to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign mentioned in the description: 15 (see page 8, line 7).

(c) They fail to comply with 37 CFR 1.84(p)(5) because they include the following reference signs not mentioned in the description: 1628, 1722, 1726, 1728, 1740, A_i, A_s, (see Figs. 18, 23, 24).

A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 7-23, 25 and 28-34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 recites an if-then clause, i.e. a conditional limitation (see lines 7-9). The claim language does not make clear whether the step set forth in this limitation is intended to be a part of the method claimed since an alternative to the condition has not been set forth, thereby rendering the claim vague and indefinite. Based on the claim language, any method which consists of the steps of providing a wafer structure, generating a signature and comparing, as recited in the claim, wherein the dimensions of the T-top gate *are* within a pre-determined acceptable range, meets the method of claim 7. That is, the claim language does not require the step of adjusting using feedback control.

Claims 8-15 include all limitations set forth in claim 7.

Claim 16 is rejected for reasons discussed above in connection with claim 7.

Claims 17-23 include all limitations set forth in claim 16.

Claim 25 recites the limitation "the T-top gate formation monitoring comprises" in lines 1-2. The limitation "the T-top gate formation monitoring" is understood as being directed to a step of a method. However, claim 24 from which claim 25 depends is directed to an in-line system for monitoring T-top gate formation. A single claim may not

be directed to both a process and a product. Therefore, the claim language of claim 25 does not make clear whether applicant intends to further limit the structure of the system set forth in claim 24 or to claim a method, thereby rendering claim 28 vague and indefinite.

Claim 28 recites the limitation "The method of claim 24" in line 1. However, claim 24 is directed to an in-line system for monitoring T-top gate formation. A single claim may not be directed to both a process and a product. Therefore, the claim language of claim 28 does not make clear whether applicant intends to further limit the structure of the system set forth in claim 24 or to claim a method, thereby rendering claim 28 vague and indefinite.

Claim 29 is rejected for the reasons discussed above in connection with claim 28.

Claim 30 recites the limitation "a scatterometry system coupled to the formation process" in line 3. It is not understood from the claim language how a system can be structurally connected to a process. Therefore, claim 30 is considered vague and indefinite.

Claims 31-33 include all limitations set forth in claim 30.

Further, Claim 33 is rejected for reasons discussed above in connection with claim 28.

Claim 34 is rejected for reasons discussed above in connection with claim 7.

Please note: For the purpose of the rejections set forth below, claims 25, 28 and 29, and claim 33 have been treated as being claims which further limit the system of claims 24 and 30, respectively.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 3-7, 9-16, 18-24, 26-29 and 34 are rejected under 35 U.S.C. 102(a) as being anticipated by U.S. Patent No. 6,270,622 to Klippert, II et al.

With regard to method claims 1, 3-7, 9-16 and 18-23, the structure of the system discussed below with respect to claims 24, 26-29 and 34 renders the steps set forth in the method claims inherent to the operation of the system.

With regard to claim 24, Klippert, II et al. disclose an in-line system for monitoring T-top gate formation comprising:

a wafer structure (see wafer) undergoing a T-top gate formation process (see recess etch process) (see Col. 7, line 66 to Col. 8, line 7);

a T-top gate formation monitoring system (see interferometry system, software program) for generating a signature associated with wafer surface dimensions during a process step (see Col. 8, lines 8-16, 32-42); and

a signature store (implied; see stored curve profile) coupled to the monitoring system, wherein the generated signature is compared to the signature store to determine a state of the T-top gate (see recess) (see Col. 8, lines 16-26).

With regard to claim 26, Klippert, II et al. teach the system of claim 24, wherein the T-top gate formation signature store comprises known signatures of wafer structures as they appear during the T-top gate formation process (see Col. 8, lines 16-26).

With regard to claim 27, Klippert, II et al. teach the system of claim 24, wherein the signature corresponds to a particular profile associated with the wafer undergoing T-top gate formation (see Col. 8, lines 16-26).

With regard to claim 28, Klippert et al. teach the system of claim 24, wherein wafer surface dimensions comprise amount of undercut and effective gate width (see Col. 8, lines 26-31).

With regard to claim 29, Klippert et al. teach the system of claim 24, comprising a feedback control system (see computer) operatively coupled to the T-top gate formation monitoring system (see Col. 8, lines 42-50).

With regard to claim 34, see discussions above with respect to claims 24 and 29.

7. Claims 1-34 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,562,248 to Subramanian et al.

The applied reference has a common assignee and inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention

disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

With regard to method claims 1-23, the structure of the system discussed below with respect to claims 24-34 renders the steps set forth in the method claims inherent to the operation of the system.

With regard to claims 24, 25, 29, 30 and 34, Subramanian et al. disclose an in-line system for determining T-top gate dimensions comprising:

a wafer structure (mask 22) undergoing a T-top gate formation process (fabrication of apertures 24) (see Fig. 7);

a signature store (memory 70) comprising known signatures associated with T-top gate formation (see Col. 10, lines 43-8, Col. 11, lines 11-4, Figs. 7, 8);

a scatterometry system (scatterometry system 51) for directing light (light 46) at and collecting reflected light (light 48) from the wafer structure (see Figs. 7, 8);

a T-top gate formation analysis system (processor 60) coupled to the scatterometry system and to the signature store for determining the T-top gate dimensions (see Col. 10, lines 26-8, Fig. 7); and

a feedback control system coupled to the T-top gate formation analysis system for optimizing T-top gate formation (see Col. 10, lines 7-12).

With regard to claims 26 and 31, Subramanian et al. teach the system of claims 24 and 30, respectively, wherein the T-top gate formation signature store comprises

known signatures of wafer structures as they appear during the T-top gate formation process (see Col. 11, lines 12-16).

With regard to claims 27 and 32, Subramanian et al. teach the system of claims 24 and 30, respectively, wherein the signature corresponds to a particular profile associated with the wafer structure undergoing T-top gate formation (see Col. 11, lines 12-16).

With regard to claims 28 and 33, Subramanian et al. teach the system of claims 24 and 30, respectively, wherein the T-top gate dimensions comprise amount of undercut and effective gate width (see Col. 10, lines 1-11).

8. Claims 1-34 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,545,753 to Subramanian et al.

The applied reference has a common assignee and inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

With regard to method claims 1-23, the structure of the system discussed below with respect to claims 24-34 renders the steps set forth in the method claims inherent to the operation of the system.

With regard to claims 24, 25, 29, 30 and 34, Subramanian et al. disclose an in-line system for determining T-top gate dimensions comprising:

a wafer structure (wafer 1010) undergoing a T-top gate formation process (formation of vias) (see Fig. 10);

a signature store (memory 1050) comprising known signatures associated with T-top gate formation (see Col. 14, lines 51-64, Fig. 10);

a scatterometry system (scatterometry system 1075) for directing light (light 630) at and collecting reflected light (light 640) from the wafer structure (see Figs. 10, 11);

a T-top gate formation analysis system (processor 1040) coupled to the scatterometry system and to the signature store for determining the T-top gate dimensions (see Fig. 10); and

a feedback control system coupled to the T-top gate formation analysis system for optimizing T-top gate formation (see Col. 15, lines 1-39).

With regard to claims 26 and 31, Subramanian et al. teach the system of claims 24 and 30, respectively, wherein the T-top gate formation signature store comprises known signatures of wafer structures as they appear during the T-top gate formation process (see Col. 14, lines 51-64, Col. 15, lines 1-39).

With regard to claims 27 and 32, Subramanian et al. teach the system of claims 24 and 30, respectively, wherein the signature corresponds to a particular profile associated with the wafer structure undergoing T-top gate formation (see Col. 14, lines 51-64, Col. 15, lines 1-39).

With regard to claims 28 and 33, Subramanian et al. teach the system of claims 24 and 30, respectively, wherein the T-top gate dimensions comprise amount of undercut and effective gate width (see Col. 12, line 60 to Col. 13, line 5, Col. 15, lines 1-39).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 2, 8, 17 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klippert, II et al. as applied to claims 1, 7, 16 and 24 above, and further in view of U.S. Patent No. 5,889,593 to Bareket.

With regard to the method claims 2, 8 and 17, the structure of the modified system of Klippert, II et al. discussed below with respect to claim 25 renders the steps set forth in the method claim inherent to the operation of the system.

With regard to claim 25, Klippert, II et al. do not teach the system of claim 24, further comprising a scatterometry system. Instead, Klippert, II et al. teach the system of claim 24 to further comprise an interferometry system (see interferometry) (see Col. 8, lines 32-42). However, Bareket teaches that it is well known in the art to use either an interferometry system or a scatterometry system for determining layer thickness and etch depth, thereby establishing such systems as art-recognized equivalents (see Col. 1, lines 20-25). Therefore, it would have been obvious to one having ordinary skill in the

art at the time the invention was made to replace the interferometry system of Klippert et al. with the scatterometry system discussed by Bareket for providing alternative means for measuring layer thickness and etch depth.

11. Claims 30-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,270,622 to Klippert, II et al. in view of U.S. Patent No. 5,889,593 to Bareket.

With regard to claim 30, Klippert, II et al. disclose an in-line system for determining T-top gate dimensions comprising:

a wafer structure (see wafer) undergoing a T-top gate formation process (see recess etch process) (see Col. 7, line 66 to Col. 8, line 7);

a signature store (implied; see stored curve profile) comprising known signatures associated with T-top gate formation (see Col. 8, lines 16-26);

an interferometry system (see interferometry) (see Col. 8, lines 32-42);

a T-top gate formation analysis system (see software program) coupled to the interferometry system and to the signature store for determining the T-top gate dimensions (see Col. 8, lines 8-31); and

a feedback control system (see computer) coupled to the T-top gate formation analysis system for optimizing T-top gate formation (see Col. 8, lines 42-50).

Klippert, II et al. do not teach a scatterometry system for directing light at and collecting reflected light from the wafer structure. Instead, Klippert, II et al. teach an interferometry system (see interferometry) (see Col. 8, lines 32-42). However, Bareket

teaches that it is well known in the art to use either an interferometry system or a scatterometry system for determining layer thickness and etch depth, thereby establishing such systems as art-recognized equivalents (see Col. 1, lines 20-25). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to replace the interferometry system of Klippert et al. with the scatterometry system discussed by Bareket for providing alternative means for measuring layer thickness and etch depth.

With regard to claim 31, Klippert, II et al. teach the system of claim 30, wherein the T-top gate formation signature store comprises known signatures of wafer structures as they appear during the T-top gate formation process (see Col. 8, lines 16-26).

With regard to claim 32, Klippert, II et al. teach the system of claim 30, wherein the signature corresponds to a particular profile associated with the wafer structure undergoing T-top gate formation (see Col. 8, lines 16-26).

With regard to claim 33, Klippert, II et al. teach the system of claim 30, wherein the T-top gate dimensions comprise amount of undercut and effective gate width (see Col. 8, lines 26-31).

Conclusion

12. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

U.S. Patent No. 6,259,521 to Miller et al.

U.S. Patent No. 5,164,790 to McNeil et al.

U.S. Patent No. 4,710,642 to McNeil

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michelle Nguyen whose telephone number is 703-305-2771. The examiner can normally be reached on M-F 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Russ Adams can be reached on 703-308-2847. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4900.

mpn
August 8, 2003

RUSSELL ADAMS
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